REMARKS

Claims 1-3, 5-12 and 14-20 were pending in the application prior to the present amendment.

Claims 5 and 20 are herein cancelled.

Claims 1, 6, 11, 16-19 are herein amended.

Claims 21 and 22 are herein added.

Thus, Claims 1-3, 6-12, 14-19 and 21-22 will be pending in the application after entry of the present amendment.

Rejection Under Section 102

Claims 1, 5 and 16-17 were rejected under 35 U.S.C. Section 102(e) as being anticipated by Horton (U.S. Patent No. 6,421,696). These rejections are respectfully traversed based on the following reasoning.

Claim 1 as amended herein recites:

> "A method of performing a two-dimensional discrete cosine transform (DCT) using a microprocessor having an instruction set that includes single-instruction multiple-data (SIMD) floating point instructions, wherein the method comprises:
>
> receiving a two-dimensional block of integer data having C columns and R rows, wherein each of the R rows contains a set of C row data values, wherein the block of integer data is indicative of a portion of an image, wherein each of C and R is an even integer; and
>
> for each row,
>
> loading the entire set of C row data values of the row into a set of C/2 registers of the microprocessor;
>
> converting the C row data values into floating point form, wherein each of the registers holds two of the floating point row data values; and
>
> performing a plurality of weighted-rotation operations on the values in the registers, wherein the weighted-rotation operations are performed using SIMD floating point instructions;
>
> altering the arrangement of values in the registers;
>
> performing a second plurality of weighted-rotation operations on the values in the registers;
>
> again altering the arrangement of the values in the registers;
>
> performing a third plurality of weighted-rotation operations on the values in the registers;

yet again altering the arrangement of the values in the registers;

performing a fourth plurality of weighted-rotation operations on the values in the registers to obtain C intermediate floating point values; and

storing the C intermediate floating point values into a next available row of an intermediate buffer."

This union of features is not taught or suggested in the cited references, whether regarded individually or in combination.

In particular, none of the cited references teach or suggest performing four pluralities of weighted-rotation operations and altering the arrangement of values in the registers between each successive plurality of weighted-rotation operations as recited in claim 1. The Examiner relies on Horton Figures 1 and 10 to provide evidence for the anticipation of this combination of features. Figure 1 illustrates multiple sets of butterfly computations organized in successive "passes". Figure 10 illustrates a single set of butterfly computations. However, these Figures do not teach or suggest rearrangements of values between pluralities of weighted rotation operations as recited in claim 1. Note that in Figure 1 the output values from the butterflies in each pass are fed directly to the inputs of the next pass without rearrangement.

Furthermore, none of the cited references teach or suggest "for each row, loading the entire set of C row data values of the row into a set of C/2 registers of the microprocessor" as recited in claim 1. The Examiner points to Horton Col. 2, lines 44-50 and Figure 6 as providing evidence for the anticipation of this feature. At Col. 2, lines 44-50, Horton recites:

"Furthermore, suppose that the input array comprises eight samples of a signal X. Thus, the eight samples may be represented as X(000), X(001), X(010), X(011), X(100), X(101), X(110) and X(111) in the order they appear in the input array. The FFT algorithm accesses these input values in the order X(000), X(100), X(010), X(110), X(001), X(101), X(011) and X(111). Coley and Tukey realized that the addresses of samples in the access order and the memory order were effectively bit reversed."

This passage in no way suggests that an entire row of data values from a received block are loaded into registers of the microprocessor as recited in claim 1. In fact, this passage never even mentions the term "register".

Horton Figure 6 illustrates a data array 700 which stores initial FFT operands and intermediate computations results as well as the final output of the FFT algorithm. However,

this Figure in no way suggests that an entire row of data values from a received block are loaded into microprocessors registers as recited in claim 1.

Thus, claim 1 and its dependents are patentably distinguished over the cited references.

Claims 16 and 17 each recite features similar to those recited in claim 1. Thus, claims 16 and 17 are patentably distinguished over the cited references at least for the reasons given above in support of claim 1.

Rejections Under Section 103

Claims 2-3 were rejected under 35 U.S.C. Section 103(a) as being obvious over Horton (U.S. Patent No. 6,421,696) in view of Advanced Micro Devices Inc. ("AMD Extensions to the 3DNow!™ and MMX™ Instructions Sets Manual").

Claims 6-12, 14-15 and 18-20 were rejected under 35 U.S.C. Section 103(a) as being obvious over Horton (U.S. Patent No. 6,421,696) in view of Hung et al. ("Statistical Inverse Discrete Cosine Transforms for Image Compression").

These rejections are respectfully traversed based on the following reasoning.

Claim 11 as amended herein recites:

> "A method of performing a discrete cosine transform (DCT) using a microprocessor having an instruction set that includes single-instruction multiple-data (SIMD) floating point instructions, wherein the method comprises:
>
> receiving a two-dimensional block of integer data having C columns and R rows, wherein each of C and R is an even integer, wherein the two-dimensional block represents a portion of an image; and
>
> for two columns at a time,
>
> loading column data from the two columns into registers of the microprocessor so that each of the registers holds one value from a first of the two columns and one value from a second of the two columns, wherein the one value from the first of the two columns and the one value from the second of the two columns are taken from the same row of the two-dimensional block;
>
> converting the column data into floating point form; and
>
> performing a plurality of weighted-rotation operations on the values in the registers, wherein the weighted-rotation operations for the two columns are performed in parallel using SIMD floating point instructions;

> as each weighted-rotation operation is done, storing weighted-rotation operation results to an intermediate buffer."

This union of features is not taught or suggested in the cited references, whether regarded individually or in combination.

In particular, none of the cited references teach or suggest:

> "for two columns at a time, loading column data from the two columns into registers of the microprocessor so that each of the registers holds one value from a first of the two columns and one value from a second of the two columns, wherein the one value from the first of the two columns and the one value from the second of the two columns are taken from the same row of the two-dimensional block"

as recited in claim 11. In the signal flow graph of Figure 2, Hung et al. (hereinafter referred to simply as "Hung") suggests operating on the odd elements and even elements of an input vector y with separate operators. However, Hung does not disclose or suggest loading two values into each register, where the two values are from different columns but from the same row of a two-dimensional input block as recited in claim 11. In fact, Hung says nothing about how the elements of input vector y are loaded into registers.

The Examiner relies on Hung Figure 4 to teach "performing a plurality of weighted-rotation operations on the values in the registers, wherein the weighted-rotation operations for the two columns are performed in parallel using SIMD floating point instructions ...". However, Hung Figure 4 merely suggests a reduction in the computations to be performed for the odd IDCT operator in the circumstance when $y(1) = y(5) = y(3) = 0$. Hung never teaches or suggests performing weighted rotation operations for two columns in parallel using SIMD floating point instructions as recited in claim 11. In fact, Applicant finds no mention of parallel operation or SIMD instructions in Hung.

Thus, Claim 11 and its dependents are patentably distinguished over the cited references.

Claims 18 and 19 each recite features similar those recited in Claim 11. Thus, Claims 18 and 19 are patentably distinguished over the cited references at least for the reasons given above in support of Claim 11.

Applicant further respectfully notes that the Horton patent (USPN 6,421,696) is not prior art to the present application under 35 U.S.C. § 103. The American Inventors Protection Act of 1999 amended 35 U.S.C. § 103(c) to state that art which qualifies as prior art only under § 102(e), (f) or (g) is not available for rejections under § 103 if that art and the subject matter of the application under examination were owned by or subject to an obligation of assignment to the same assignee at the time the invention was made. This change to 35 U.S.C. § 103(c) is effective for any application filed on or after November 29, 1999. The present application is an application for patent filed after November 29, 1999. At the time the invention was made, the subject matter of present application and the Horton patent were both owned by or subject to an obligation of assignment to the same assignee, Advanced Micro Devices, Inc.., as evidenced by

(a) the assignment for the present application recorded in the PTO at reel 011550, frame 0050, and

(b) the assignment for the Horton patent recorded in the PTO at reel 010186, frame 0417.

Therefore, the amendment to 35 U.S.C. § 103(c) made by the American Inventors Protection Act of 1999 applies to the present application and operates to exclude the Horton patent as available prior art for rejections under 35 U.S.C. § 103.

CONCLUSION

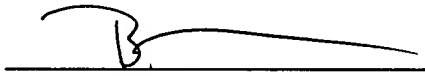
Applicant submits that the application is in condition for allowance, and an early notice to that effect is requested. If any extensions of time (under 37 C.F.R. § 1.136) are necessary to prevent the above referenced application(s) from becoming abandoned, Applicant hereby petitions for such extensions. If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert & Goetzel, P.C. Deposit Account No. 501505/5500-60900/BNK.

Also enclosed herewith are the following items:

☒ Return Receipt Postcard

☐ Fee Authorization Form authorizing a deposit account debit in the amount of $___ for fees ( ).

Respectfully submitted,



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